WHAT IS CLAIMED IS:

1. A process for sampling the signal delivered by an active pixel of an image sensor comprising a phase of storage of the signal in a pair of sampling capacitors comprising two successive respective effective electrical links of the two sampling capacitors with a follower transistor tracking the pixel in the course of the two respective sampling pulses corresponding respectively to two successive different levels of pixel voltage that are applied to a gate of the follower transistor, wherein the process for the storage phase comprises for each sampling capacitor:

applying to this sampling capacitor a voltage equal to the corresponding pixel voltage minus the gate-source voltage of the follower transistor biased with a predetermined constant bias current for a first predetermined duration so as to obtain for the said sampling capacitor a final state of stable charge;

interrupting the bias current; and

ending the sampling pulse on completion of a second predetermined duration after the said interruption of the current.

2. The process according to Claim 1, wherein the second duration is chosen in such a way as to obtain at the end of the said sampling pulse, a residual current flowing through the follower transistor less than a predetermined threshold corresponding to a predetermined threshold level of the noise of the follower transistor.

3. The process according to Claim 2, wherein the predetermined threshold level for the noise of the follower transistor lies between approximately 50 and 100 microvolts.

4. The process according to Claim 1, wherein the first duration is a fraction of the duration of the said sampling pulse, the bias current then being greater than a predetermined threshold.

5. The process according to Claim 4, wherein the duration of the sampling pulse is of the order of one microsecond, the first duration is of the order of 100 nanoseconds, and the bias current is of the order of 10 microamperes.

6. The process according to Claim 1, wherein each sampling capacitor is precharged to a predetermined initial value before each sampling pulse.

7. An image sensor, comprising:

a matrix of active pixels;

means for processing information delivered by the matrix of active pixels, the processing means comprising:

a pair of sampling capacitors per column of the matrix that are able to be respectively linked electrically to a follower transistor tracking each pixel of the column in the course of two respective sampling pulses corresponding respectively to two successive different levels of pixel voltage that are applied to a gate of the follower transistor;

a current source connected to each column of the matrix, and able to deliver on command to the column a predetermined constant bias current; and

control means operable for each sampling capacitor and in the course of the corresponding sampling pulse to:

energize the column with the bias current for a first predetermined duration so as to obtain for the said sampling capacitor a final state of stable charge;

interrupt the energizing of the column by the bias current; and

end the sampling pulse on completion of a second predetermined duration after the interruption of the current.

8. The sensor according to Claim 7, wherein the second duration is chosen in such a way as to obtain at the end of the sampling pulse, a residual current flowing through the follower transistor less than a predetermined threshold corresponding to a predetermined threshold level of the noise of the follower transistor.

9. The sensor according to Claim 8, wherein the predetermined threshold level for the noise of the follower transistor lies between approximately 50 and 100 microvolts.

10. The sensor according to Claim 7, wherein the first duration is a fraction of the duration of the sampling pulse, the bias current then being greater than a predetermined threshold.

11. The sensor according to Claim 10, wherein the duration of the sampling pulse is of the order of one microsecond, the first duration is of the order of 100 nanoseconds, and the bias current is of the order of 10 microamperes.

12. The sensor according to Claim 7, wherein the current source is connected to the said column by an interrupter controllable by the control means.

13. The sensor according to Claim 7, wherein the processing means comprise precharging means able to precharge each sampling capacitor to a predetermined initial value before each sampling pulse.

14. The sensor according to Claim 13, wherein each sampling capacitor possesses a terminal linked to ground, and the precharging means comprise two additional controllable interrupters able to link respectively the other two terminals of the two sampling capacitors to ground.

15. A circuit, comprising:

a pixel sensor;

a transistor coupling the pixel sensor to a bit line;

a first sampling capacitor selectively coupled to the bit line;

a second sampling capacitor selectively coupled to the bit line;

a bias current generator selectively coupled to the bit line;

a control circuit operable to selectively couple the bit line to the first sampling capacitor during a first sample period and selectively couple the bit line to the second sampling capacitor during a second sample period, the control circuit further operable, during each of the first and second sample periods, to selectively couple the bias current generator to the bit line to bias the transistor into a follower configuration.

16. The circuit of claim 15 wherein the control circuit selectively couples the bias current generator to the bit line at a beginning of each of the first and second sample periods.

17. The circuit of claim 16 wherein the control circuit de-couples the selectively coupled bias current generator from the bit line before an end of each of the first and second sample periods.

18. The circuit of claim 17, wherein each first and second sampling period is of the order of one microsecond, and a duration of the selective coupling of the bias current generator is of the order of 100 nanoseconds.

19. A method for capacitively sampling a pixel sensor coupled to a bit line through a transistor, comprising:

initiating a sample period by applying a bias current to the bit line and coupling the bit line to a sensing capacitor;

after a first time period, terminating application of the bias current; and

after a subsequent second time period decoupling the sensing capacitor from the bit line to terminate the sample period.

20. The method of claim 19 wherein the bias current biases the transistor into a follower configuration.

21. The method of claim 19 wherein a length of the first time period is chosen to allow the sensing capacitor to reach a substantially stable charge state.

22. The method of claim 21 wherein the length of the first time period is approximately 100 nanoseconds.

23. The method of claim 19 wherein the bias current has a value on the order of 10 micro-amperes.

24. The method of claim 19 wherein the sample period has a length on the order of about one microsecond.

25. The method of claim 19 further comprising:

performing the initiating, terminating and decoupling operations to measure an initial pixel voltage; and

repeating the initiating, terminating and decoupling operations to measure a final pixel voltage.

26. A circuit, comprising:

a pixel sensor;

a transistor coupling the pixel sensor to a bit line;

a sampling capacitor selectively coupled to the bit line;

a bias current generator selectively coupled to the bit line;

a control circuit operable to selectively couple the bit line to the sampling capacitor during a sample period, the control circuit further operable to selectively couple the bias current generator during the sample period to the bit line to bias the transistor into a follower configuration.

27. The circuit of claim 26 wherein the control circuit selectively couples the bias current generator to the bit line at a beginning of the sample period.

28. The circuit of claim 27 wherein the control circuit de-couples the selectively coupled bias current generator from the bit line before an end of the sample period.

29. The circuit of claim 28, wherein the sampling period is of the order of one microsecond, and a duration of the selective coupling of the bias current generator is of the order of 100 nanoseconds.